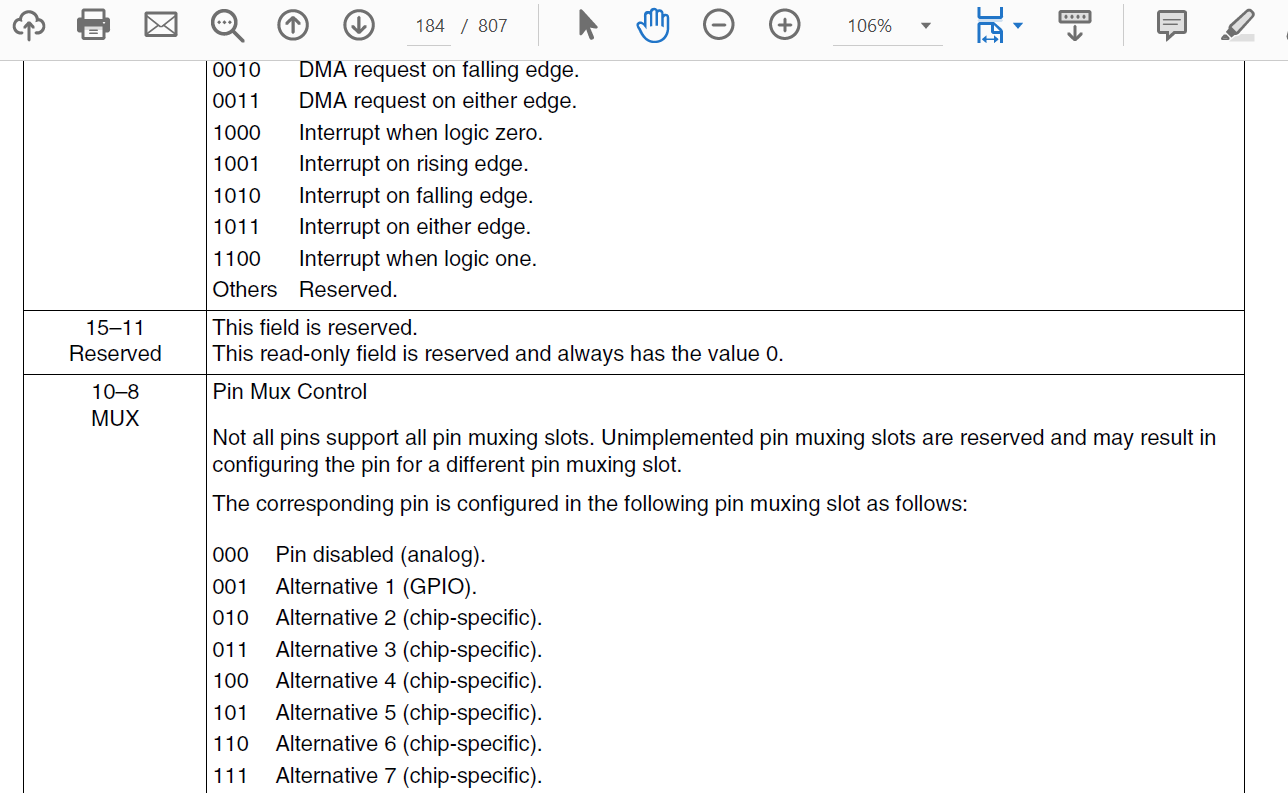
**CG2271 Lab 4 Report**

1. The purpose is to enable the clock signal in Port B.

2. To make pin 0 and 1 GPIOs.

3. Value 3 is used to select the chip-specific alternative 3, toggling TPM1\_CH0 and TPM1\_CH1.



A close up of a piece of paper

Description automatically generated

4. To enable the clock for timer 1 (TPM1).

5.

The first line clears the SOPT2 to 0.

The second line selects the TPM clock source. Since 1 is selected, either MCGFLLCLK clock or MCGFLLCLK/2 is used.

6. It is to enable prescaler and clock mode selection. The second line shows that LPTPM counter will increment on every LPTPM counter clock and that prescaler of 128 is chosen. The last line select sets LPTPM counter to operate in up counting mode.

7.

The first line resets TPM1\_C0SC to ‘0’s and disables all the channels.

ELSB is set to 1, while ELSA remains at 0, MSB is set to 1 while MSA is set to 0, thus it is selecting the mode – Edge-aligned PWM for high-true pulses (Clear output on match, set output on reload).

8.

MOD value = 48 MHz / (128\*50) = 7500  
C0V value = MOD / 2 = 7500 / 2 = 3750.